Low Skew, 1-TO-24 Differential-to LVCMOS Fanout Buffer

8344

DATASHEET

General Description

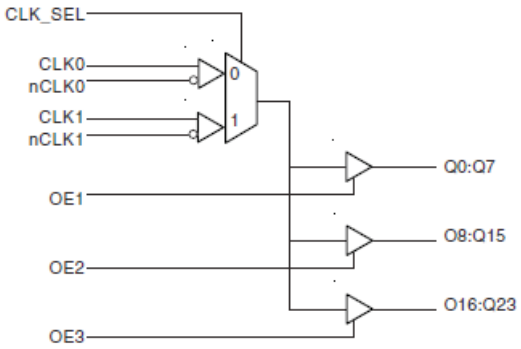
The 8344 is a low voltage, low skew, 1-to-24 Differential-to-LVCMOS Fanout Buffer. The 8344 is designed to translate any differential signal levels to LVCMOS levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. 8344 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the 8344 ideal for those clock distribution applications demanding well defined performance and repeatability.

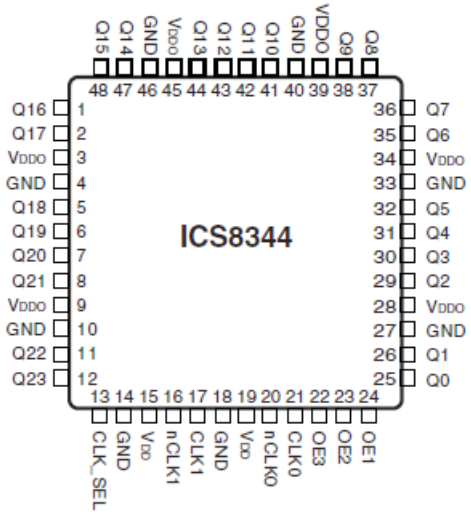
Features

- Twenty-four LVCMOS outputs, 7Ω typical output impedance
- Selectable differential clock input pairs for redundant clock applications
- CLKx, nCLKx pairs can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: 167MHz
- Translates any differential input signal (LVPECL, LVHSTL, LVDS) to LVCMOS without external bias networks
- Translates any single-ended input signal to LVCMOS with resistor bias on nCLK input
- Multiple output enable pins for disabling unused outputs in reduced fanout applications
- Output skew: 275ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Bank skew: 150ps (maximum)
- Propagation Delay: 4.3ns (maximum)
- 3.3V, 2.5V or mixed 3.3V, 2.5V operating supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



48-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q15 thru Q23 outputs. 7Ω typical output impedance.
3, 9, 28, 34, 39, 45	V_{DDO}	Power		Output supply pins. Connect 3.3V or 2.5V.
4, 10, 14,18, 27, 33, 40, 46	GND	Power		Power supply ground. Connect to ground.
13	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs.
15, 19	V_{DD}	Power		Positive supply pins. Connect 3.3V or 2.5V.
16	nCLK1	Input	Pullup	Inverting input of secondary differential clock input pair.
17	CLK1	Input	Pulldown	Non-inverting input of secondary differential clock input pair.
20	nCLK0	Input	Pullup	Inverting input of primary differential clock input pair.
21	CLK0	Input	Pulldown	Non-inverting input of primary differential clock input pair.
22	OE3	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q16 thru Q23.
23	OE2	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q8 thru Q15.
24	OE1	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q7.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Q0 thru Q7 outputs. 7Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Q8 thru Q15 outputs. 7Ω typical output impedance.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V				pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V				pF
		V_{DD}, V_{DDO} = 2.625V				pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	**Output**	**Input**	**Output**	**Input**	**Output**
OE1	**Q0-Q7**	**OE2**	**Q8-Q15**	**OE3**	**Q16-Q23**
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Active	1	Active	1	Active

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	**CLK0, nCLK0**	**CLK1, nCLK1**
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUTS FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE1, OE2, OE3	**CLK**	**nCLK**	**Q0 thru Q23**		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Absolute Maximum Ratings

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Positive Supply Current				120	mA

Table 4B. LVCMOS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 3.465V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 3.465$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 3.465$, $V_{IN} = 0$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO} = 3.135V$ $I_{OH} = -36mA$	2.6			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO} = 3.135V$ $I_{OL} = 36mA$			0.6	V

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; Note 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				167	MHz
tp_{LH}	Propagation Delay Low-to-High; NOTE 1	f ≤ 167MHz	2.6		4.3	ns
tp_{HL}	Propagation Delay High-to-Low; NOTE 1	f ≤ 167MHz	2.4		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Measured on the rising edge of $V_{DDO}/2$			150	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on the rising edge of $V_{DDO}/2$			275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on the rising edge of $V_{DDO}/2$			600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	200		1000	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	200		1000	ps
t_{PW}	Output Pulse Width	f ≤ 167MHz	tPeriod/2 - 0.65	tPeriod/2	tPeriod/2 + 0.65	ns
		f = 167MHz	2.35	2.5	3.65	ns
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			5	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			4	ns

All parameters measured at 167MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Positive Supply Current				120	mA

TABLE 4E. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	V_{DD} = 3.465, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465, V_{IN} = 0	-5			µA
V_{OH}	Output High Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OH} = -27mA	1.8			V
V_{OL}	Output Low Voltage		V_{DD} = 3.135V V_{DDO} = 2.375V I_{OL} = 27mA			0.63	V

TABLE 4F. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; Note 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				167	MHz
tp_{LH}	Propagation Delay Low-to-High; NOTE 1	f ≤ 167MHz	2.6		4.5	ns
tp_{HL}	Propagation Delay High-to-Low; NOTE 1	f ≤ 167MHz	2.6		4.2	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Measured on the rising edge of $V_{DDO}/2$			150	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on the rising edge of $V_{DDO}/2$			275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on the rising edge of $V_{DDO}/2$			600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
t_{PW}	Output Pulse Width	f ≤ 167MHz	tPeriod/2 - 0.65	tPeriod/2	tPeriod/2 + 0.65	ns
		f = 167MHz	2.35		3.65	ns
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

All parameters measured at 167MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Positive Supply Current				120	mA

TABLE 4H. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL, OE1, OE2, OE3		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL, OE1, OE2, OE3		-0.3		0.8	V
I_{IH}	Input High Current	OE1, OE2, OE3	$V_{DD} = V_{IN} = 2.625V$			5	µA
		CLK_SEL	$V_{DD} = V_{IN} = 2.625V$			150	µA
I_{IL}	Input Low Current	OE1, OE2, OE3	$V_{DD} = 2.625V$, $V_{IN} = 0V$	-150			µA
		CLK_SEL	$V_{DD} = 2.625V$, $V_{IN} = 0$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO} = 2.375V$ $I_{OH} = -27mA$	1.77			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO} = 2.375V$ $I_{OL} = 27mA$			0.6	V

TABLE 4I. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1				5	µA
		CLK0, CLK1				150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1		-150			µA
		CLK0, CLK1		-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; Note 1, 2			GND + 0.5		V_{DD} - 0.85	V

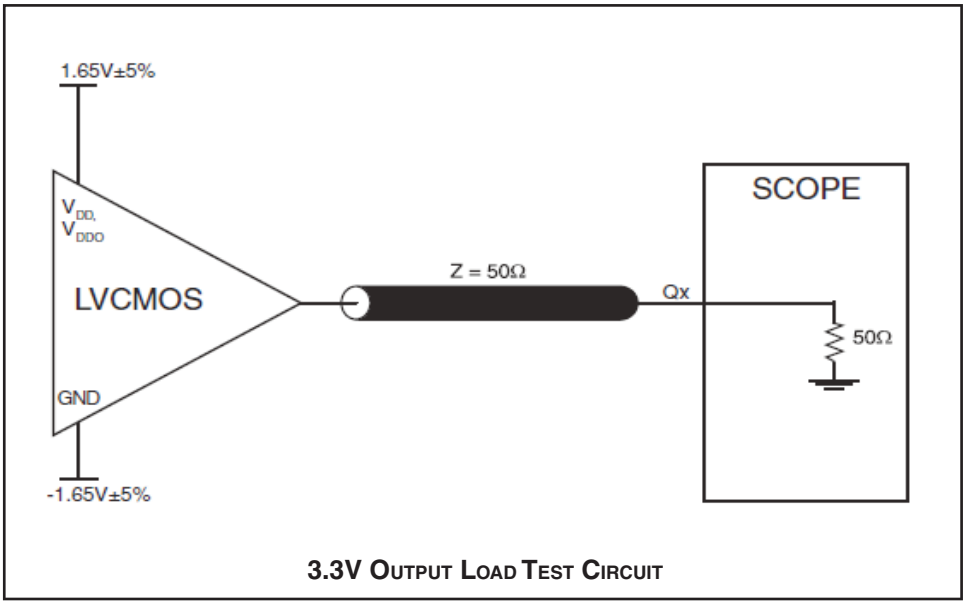
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

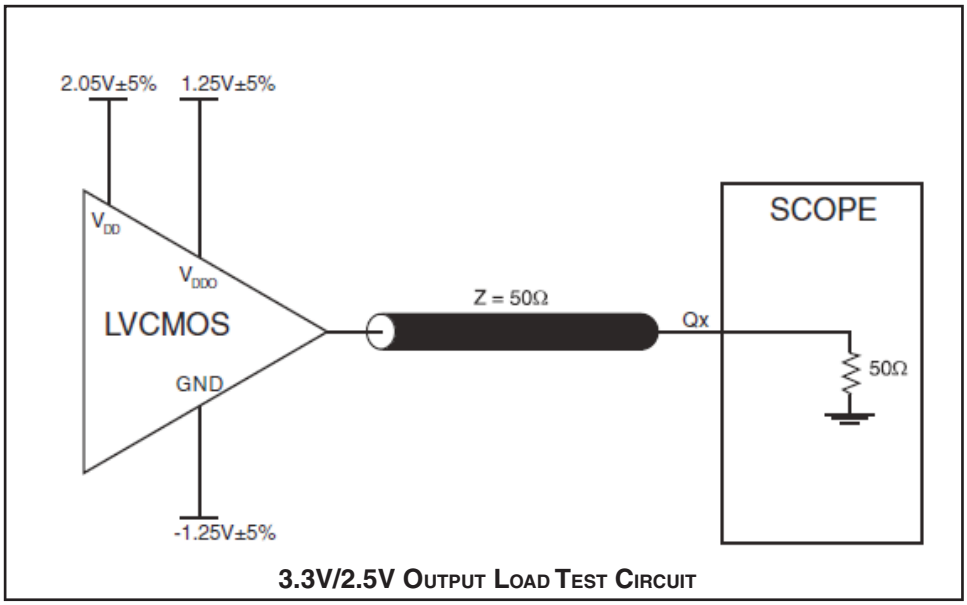
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				167	MHz
tp_{LH}	Propagation Delay Low-to-High; NOTE 1	f ≤ 167MHz	2.7		4.3	ns
tp_{HL}	Propagation Delay High-to-Low; NOTE 1	f ≤ 167MHz	2.7		4.3	ns
*t*sk(b)	Bank Skew; NOTE 2, 6	Measured on the rising edge of $V_{DDO}/2$			150	ps
*t*sk(o)	Output Skew; NOTE 3, 6	Measured on the rising edge of $V_{DDO}/2$			275	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6	Measured on the rising edge of $V_{DDO}/2$			600	ps
t_R	Output Rise Time; NOTE 5	30% to 70%	300		1700	ps
t_F	Output Fall Time; NOTE 5	30% to 70%	300		1400	ps
t_{PW}	Output Pulse Width	f ≤ 167MHz	tPeriod/2 - 0.65	tPeriod/2	tPeriod/2 + 0.65	ns
		f = 167MHz	2.35		3.65	ns
t_{EN}	Output Enable Time; NOTE 5	f = 66.7MHz			6	ns
t_{DIS}	Output Disable TIme; NOTE 5	f = 66.7MHz			6	ns

All parameters measured at 167MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 4: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

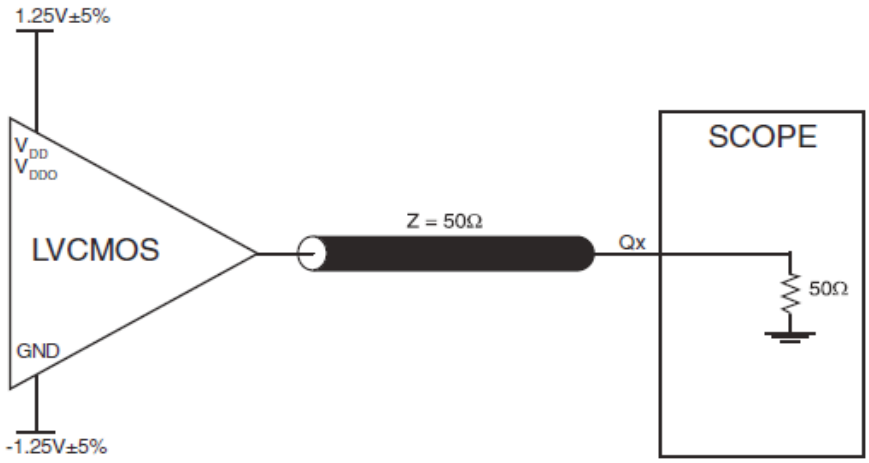
Parameter Measurement Information



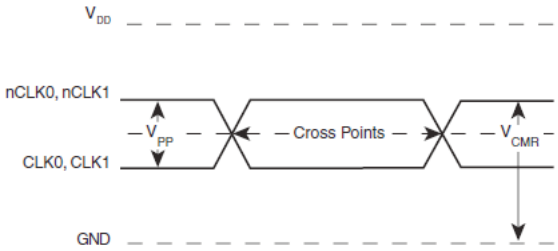
3.3V Output Load Test Circuit



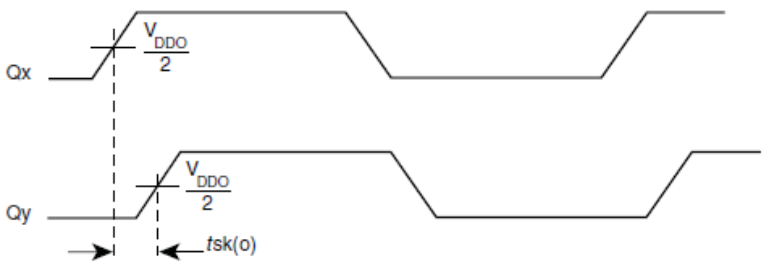
3.3V/2.5V Output Load Test Circuit



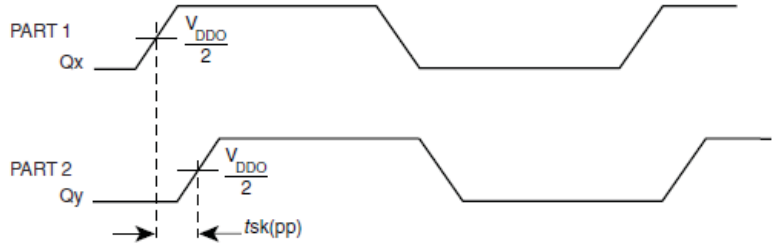
2.5V Output Load Test Circuit



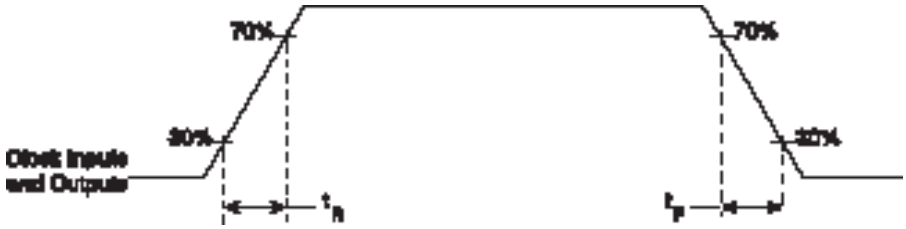
Differential Input Level



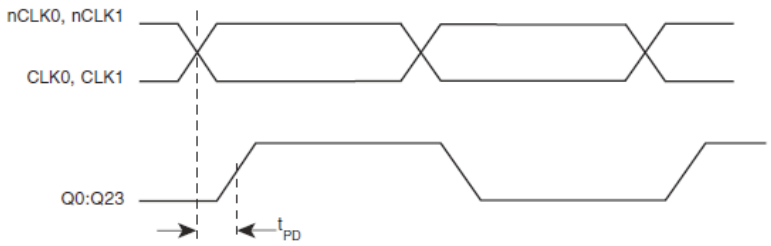
Output Skew



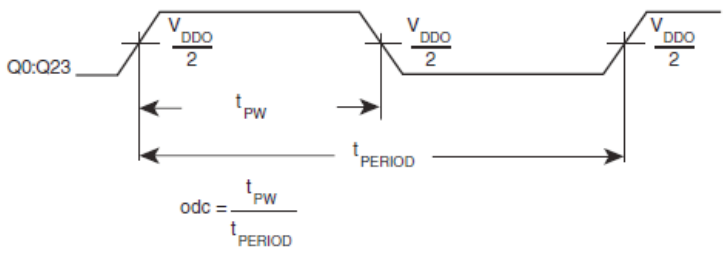
PART-TO-PART SKEW



INPUT AND OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



t_{PW} & t_{PERIOD}

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

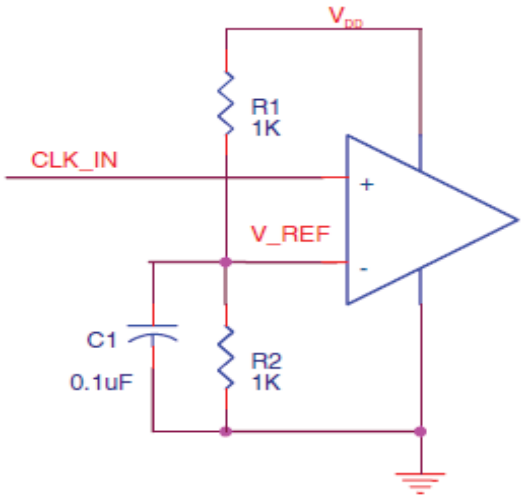


Figure 1 - Single Ended Signal Driving Differential Input

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: For 48-pin LQFP

Transistor Count

The transistor count for 8344 is: 1449

Package Outline - Y Suffix

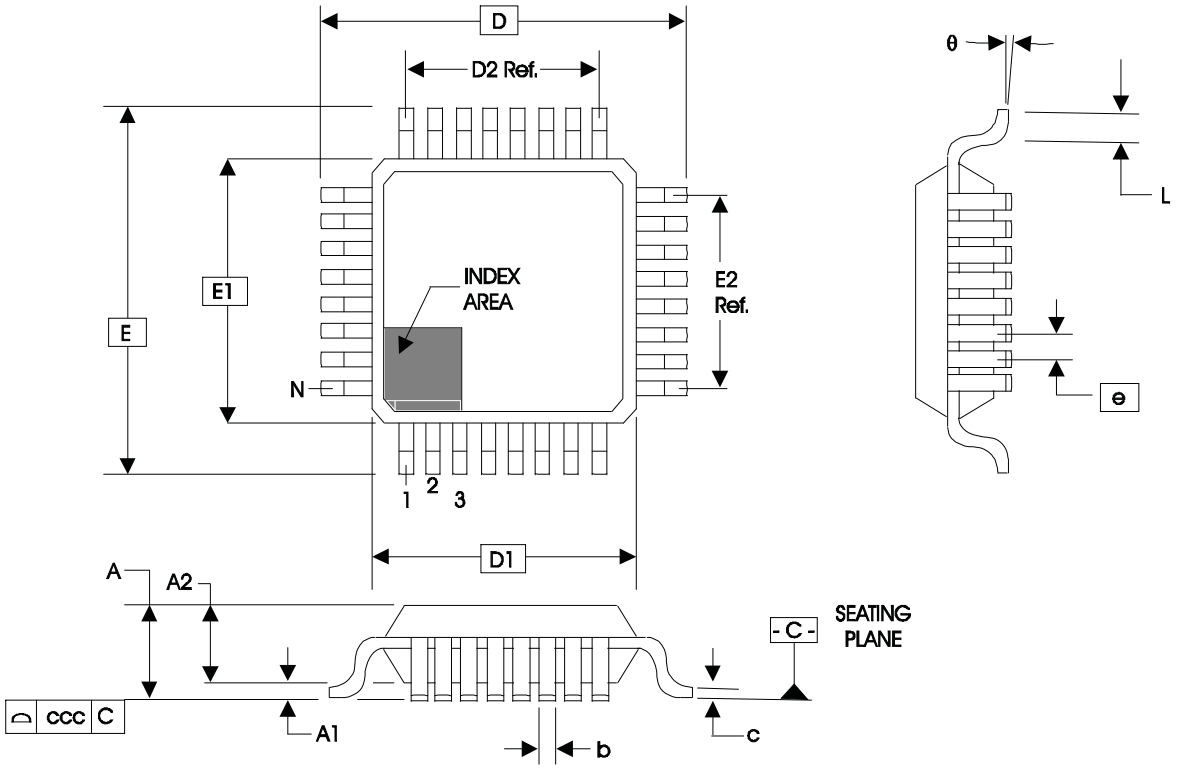


Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8344BYLF	ICS8344BYLF	Lead-Free, 48 Lead LQFP	Tray	0°C to 70°C
8344BYLFT	ICS8344BYLF	Lead-Free, 48 Lead LQFP	Tape and Reel	0°C to 70°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	1 16	Features Section - added lead-free bullet. Ordering Information Table - deleted “ICS” prefix from Part/Order column. Added lead-free marking. Updated Header/Footer with IDT.	1/5/11
A	T8	15	Ordering Information - removed leaded devices. Updated Datasheet format.	3/24/15

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